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DAHIMENE, MAHMOUD	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/689,617	OKAMOTO, SATORU	
	Examiner	Art Unit	
	Mahmoud Dahimene	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-95* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *85-95* is/are allowed.

6)☒ Claim(s) *1-84* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. Rejection of claim 1 under 35 U.S.C. 112, first paragraph is withdrawn in view of applicant's remark clarifying the limitation "not to form a semiconductor device" is interpreted as "using a dummy substrate".

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1-5, 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow et al. (US 6,872,322) in view of Lui et al. (US 6,566,270) and Wolf (Silicon Processing for the VLSI Era, Volume 4- Deep Submicron Process Technology, Lattice Press, 2002, page 11).

Regarding claim 1, Chow discloses a method for cleaning a chamber with a plasma including the steps ofsteps of: forming a polysilicon/semiconductor film over a substrate and a tungsten silicide /conductive layer over the semiconductor film (col 11, lines 1-3); filling a chamber with CI2 and generating plasma from the CI2 to clean the

chamber (col 11, lines 35-42); placing the wafer/substrate with the polysilicon/semiconductor film and a tungsten silicide/conductive layer in the chamber being cleaned with added cleaning gas/cleaned chamber to etch the conductive film in the cleaned chamber by repeating the etching steps (col 10, lines 52-57; col 11, lines 1-20; fig. 3).

Chow discloses forming a silicon oxide layer under the polysilicon and tungsten layers (col 8, lines 15-17). The oxide layer of Chow is a gate oxide deposited on top of a semiconductor film which forms the channel underneath the gate, as anyone with ordinary skill in the art would know that the semiconducting channel is formed on a "first" substrate. It is noted that Chow is silent about the formation of the transistor channel including the oxide layer being deposited on a conductive layer, however Wolf teaches p-wells or n-wells are conventionally used in device formation see figure 1-7 of Wolf (page 11). One of ordinary skill in the art would have been motivated to use p-wells or n-wells in order to form a twin-well CMOPS structure as suggested by Wolf.

Chow discloses the use of dummy wafers/substrates for seasoning the chamber, however, it is noted that Chow is silent about using a second substrate which is not to form a device (conventionally known as a dummy substrate) for cleaning the chamber.

Lui discloses dummy substrates are conventionally used for etch chamber cleaning (column 1, line 33).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Chow to use a dummy substrate because dummy substrates are conventionally used for etch chamber cleaning. One of

ordinary skill in the art would have been motivated to use a dummy substrate in order to decouple the process of chamber cleaning from the process of etching when the substrate is sensitive to the cleaning byproducts. One of ordinary skill in the art would have been motivated to modify the method of Chow by performing cleaning independently of the etching step when the cleaning process result in undesirable effects on the substrate such as contamination or incontrollable etch, the method of Chow could obviously be extended to process more delicate substrates, by performing independent etch and clean steps. Lui teaches cleaning the chamber using a dummy wafer on the chuck while cleaning.

Applicant does not specify what specific kind of etching in performed, it would appear that the chamber cleaning procedure and the etch step of Chow would be effective regardless of whether an insulating layer is present under the conducting layer or not, etching is usually performed on the topmost layer. It would also appear obvious to one of ordinary skill in the art at the time the invention was made that the sequence of layers positioned bellow the topmost layers of conductive films would not affect the chamber cleaning step since those layers are not exposed to the cleaning environment. Chow teaches the general concept of chamber cleaning for the purpose of increasing etch selectivity by reducing the concentration of unwanted species released from deposits on the chamber walls from a previous etch process performed within the same chamber.

Regarding claim 2, Chow discloses using an ICP etching method (col 6, lines 35-40)

Regarding claim 3, Chow discloses that the fluorine gas is CF4 (col 9, lines 37-40),

As to claim 4, it is noted that Chow is silent about a glass or quartz dummy wafer for the cleaning step, however, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Chow to use a dummy substrate made of any material including glass or quartz wich is compatible with the chamber and process chemistry because a dummy wafer is used only during cleaning. One of ordinary skill in the art would have been motivated to use glass or quartz in order to prevent introducing impurities in the chamber since glass or quartz (SiO2) is conventionally used as a material for material fill or gate material, also quartz is resistant to the cleaning chemistry, and glass or quartz wafers are readily available as dummy wafers.

Regarding claims 5, Chow discloses adding oxygen gas to the cleaning plasma (col 9, lines 37-40), and cites "The present process allows etching of one or more layers on a substrate 25 and simultaneous cleaning of the plasma etching chamber 30 in which the etching process is performed, without stopping the etching process. In one or more of the etch process stages, a cleaning gas is added to the etchant gas in a volumetric ratio selected so that the etching residue formed in any one of the etching stages; or the residue formed in all of the etching stages is substantially entirely removed during the etching process. The etchant gas comprises one or more of Cl.sub.2, N.sub.2, O.sub.2, HBr, or He--O.sub.2 ; and the cleaning gas comprises one or more of NF.sub.3, CF.sub.4, or SF.sub.6. It has been discovered that

combinations of these gases provide unique and unexpected etching and cleaning properties" (colum 9, lines 1-14). Chow teaches that it has been discovered that combinations of these gases provide unique and unexpected etching and cleaning properties, it would have been obvious to one of ordinary skill in the art at the time the invention was made to remove the etching component of the gas mixture during cleaning step while keeping the cleaning component of the gas mixture.

As to claim 7, fig. Id of Chow shows an island shaped semiconductor structure is formed.

Claim Rejections - 35 USC § 103

3. Claims 8-13, 22-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow et al. (US 6,872,322) in view of Lui et al. (US 6,566,270) and Wolf (Silicon Processing for the VLSI Era, Volume 4- Deep Submicron Process Technology, Lattice Press, 2002, page 11).

Regarding claims 8, 22, 27, the references of Chow, Lui and Wolf have been discussed above.

Chow discloses a method for plasma cleaning a plasma etching chamber comprising the steps of:

placing a substrate having a first polysilicon layed conductive film and a second conductive film of tungsten silicide over the first conductive film within a chamber (col 11, lines 1-3)

etching the first conductive film and the second conductive film within the chamber

using an etching gas and cleaning the chamber with a plasma generated from Cl2 or a mixed gas of Cl2 and a fluorine-based gas after the first conductive film and the second conductive film have been etched, etching the second conductive film within the cleaned chamber by repeating the etching step (col 10, lines 52-57; col 11, lines 1-20; fig. 3).

It is noted that Chow discloses the use of dummy wafers/substrates for seasoning the chamber, however, it is noted that Chow is silent about using a second substrate which is not to form a device conventionally known as a dummy substrate for cleaning the chamber.

Lui discloses dummy substrates are conventionally used for etch chamber cleaning (column 1, line 33).

Chow discloses forming a silicon oxide layer under the polysilicon and tungsten layers (col 8, lines 15-17). The oxide layer of Chow is a gate oxide deposited on top of a semiconductor film which forms the channel underneath the gate, as anyone with ordinary skill in the art would know that the semiconducting channel is formed on a "first" substrate It is noted that Chow is silent about the formation of the transistor channel including the oxide layer being deposited on a conductive layer, however Wolf teaches p-wells or n-wells are conventionally used in device formation see figure 1-7 of Wolf (page 11). One of ordinary skill in the art would have been motivated to use p-wells or n-wells in order to form a twin-well CMOPS structure as suggested by Wolf.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Chow to use a dummy substrate because dummy substrates are conventionally used for etch chamber cleaning. One of ordinary skill in the art would have been motivated to use a dummy substrate in order to decouple the processes of chamber cleaning from etching when the substrate is sensitive to the cleaning byproducts.

Applicant does not specify what specific kind of etching in performed, it would appear that the chamber cleaning procedure and the etch step of Chow would be effective regardless of whether an insulating layer is present under the conducting layer or not, etching is usually performed on the topmost layer. It would also appear obvious to one of ordinary skill in the art at the time the invention was made that the sequence of layers positioned bellow the topmost layers of conductive films would not affect the chamber cleaning step since those layers are not exposed to the cleaning environment. Chow teaches the general concept of chamber cleaning for the purpose of increasing etch selectivity by reducing the concentration of unwanted species released from deposits on the chamber walls from a previous etch process performed within the same chamber.

Regarding claims 9, 23, Chow discloses using an ICP etching method (col 6, lines 35-40)

Regarding claim 10, 24, Chow discloses that the fluorine gas is CF4 (col 9, lines 37- 40)

Regarding claims 11, 13, 25, 28, it is noted that Chow is silent about a glass or quartz dummy wafer for the cleaning step, however, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Chow to use a dummy substrate made of any material including glass or quartz wich is compatible with the chamber and process chemistry because a dummy wafer is used only during cleaning. One of ordinary skill in the art would have been motivated to use glass or quartz in order to prevent introducing impurities in the chamber since glass or quartz (SiO2) is conventionally used as a material for material fill or gate material, also quartz is resistant to the cleaning chemistry, and glass or quartz wafers are readily available as dummy wafers.

Regarding claims 12, 26, 27 Chow discloses adding oxygen gas to the cleaning plasma (col 9, lines 37-40) and cites "The present process allows etching of one or more layers on a substrate 25 and simultaneous cleaning of the plasma etching chamber 30 in which the etching process is performed, without stopping the etching process. In one or more of the etch process stages, a cleaning gas is added to the etchant gas in a volumetric ratio selected so that the etching residue formed in any one of the etching stages; or the residue formed in all of the etching stages is substantially entirely removed during the etching process. The etchant gas comprises one or more of Cl.sub.2, N.sub.2, O.sub.2, HBr, or He--O.sub.2 ; and the cleaning gas comprises one or more of NF.sub.3, CF.sub.4, or SF.sub.6. It has been discovered that combinations of these gases provide unique and unexpected etching and cleaning properties" (colum 9, lines 1-14). Chow teaches that it has been discovered that

combinations of these gases provide unique and unexpected etching and cleaning properties, it would have been obvious to one of ordinary skill in the art at the time the invention was made to remove the etching component of the gas mixture during cleaning step while keeping the cleaning component of the gas mixture.

Claim Rejections - 35 USC § 103

4. Claims 15-19, 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow et al. (US 6,872,322) in view of Lui et al. (US 6,566,270) and Wolf (Silicon Processing for the VLSI Era, Volume 4- Deep Submicron Process Technology, Lattice Press, 2002, page 11).

The references of Chow, Lui and Wolf have been discussed above.

Chow discloses a method for cleaning a plasma etching chamber comprising the steps of:

placing a substrate having a conductive film of tungsten silicide within a chamber (col 11, lines 1-3),

cleaning the chamber with a plasma generated from CI2, etching the conductive film within the cleaned chamber by repeating the etching step (col 10, lines 52-57; col 11, lines 1-20; fig. 3), Chow discloses that the fluorine gas is CF4 (col 9, lines 37-40)

Chow discloses forming a silicon oxide layer under the polysilicon and tungsten layers (col 8, lines 15-17).

Chow discloses forming a silicon oxide layer under the polysilicon and tungsten layers (col 8, lines 15-17). The oxide layer of Chow is a gate oxide deposited on top of a semiconductor film which forms the channel underneath the gate, as anyone with ordinary skill in the art would know that the semiconducting channel is formed on a "first" substrate. It is noted that Chow is silent about the formation of the transistor channel including the oxide layer being deposited on a conductive layer, however Wolf teaches p-wells or n-wells are conventionally used in device formation see figure 1-7 of Wolf (page 11). One of ordinary skill in the art would have been motivated to use p-wells or n-wells in order to form a twin-well CMOPS structure as suggested by Wolf.

It is noted that Chow discloses the use of dummy wafers/substrates for seasoning the chamber, however, Chow is silent about using a second substrate which is not to form a device conventionally known as a dummy substrate for cleaning the chamber.

Lui discloses dummy substrates are conventionally used for etch chamber cleaning (column 1, line 33).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Chow to use a dummy substrate because dummy substrates are conventionally used for etch chamber cleaning. One of ordinary skill in the art would have been motivated to use a dummy substrate in order to decouple the processes of chamber cleaning from etching when the substrate is sensitive to the cleaning byproducts. One of ordinary skill in the art would have been motivated to modify the method of Chow by performing cleaning independently of the

etching step when the two processes result in undesirable effects on the substrate such as contamination or incontrollable etch, the method of Chow could obviously be extended to process more delicate substrates, by performing independent etch and clean steps.

Applicant does not specify details on the kind of etching performed in applicant's claim 15, it would appear that the chamber cleaning procedure and the etch step of Chow would be effective regardless of whether an insulating layer is present under the conducting layer or not, etching is usually performed on the topmost layer. It would also appear obvious to one of ordinary skill in the art at the time the invention was made that the sequence of layers positioned bellow the topmost layers of conductive films would not affect the chamber cleaning step since those layers are not exposed to the cleaning environment.

Regarding claim 16, Chow discloses using an ICP etching method (col 6, lines 35- 4O)

Regarding claim 17, Chow discloses that the fluorine gas is CF4 (col 9, lines 37-40)

The limitation of claim 18 has been discussed above

Regarding claim 19, Chow discloses adding oxygen gas to the cleaning plasma (col 9, lines 37-40)

Regarding claim 21, Chow discloses using a etching gas mixture of Cl2, SF6 and oxygen (col 9, lines 36-51)

Claim Rejections - 35 USC § 103

5. Claims 29-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow et al (US 6,872,322) in view of Ye et al (US 5,756,400) and of Lui et al. (US 6,566,270) and Wolf (Silicon Processing for the VLSI Era, Volume 4- Deep Submicron Process Technology, Lattice Press, 2002, page 11).

6. The references of Chow, Lui and Wolf have been discussed above.

Regarding claims 29, 35, Chow discloses a method for cleaning a plasma etching chamber comprising the steps of:

filling the chamber with CI2 and generating plasma from the CI2 to clean the chamber (col 11, lines 35-40), a ceiling of the chamber is made of transparent dielectric material, the ceiling is exposed to the inside of the chamber (col 6, lines 29-32; fig. 2), which reads on a exposed part of the chamber is made from quartz, applying a dielectric magnetic field through the ceiling/quarts and the electrode to generate plasma (col 6, lines 30-54), etching residues are adhered to the chamber surface that includes the ceiling/quartz surface (col 11, lines 40-42).

Chow discloses forming a silicon oxide layer under the polysilicon and tungsten layers (col 8, lines 15-17).

Chow discloses forming a silicon oxide layer under the polysilicon and tungsten layers (col 8, lines 15-17). The oxide layer of Chow is a gate oxide deposited on top of a semiconductor film which forms the channel underneath the gate, as anyone with ordinary skill in the art would know that the semiconducting channel is formed on a "first" substrate. It is noted that Chow is silent about the formation of the transistor

channel including the oxide layer being deposited on a conductive layer, however Wolf teaches p-wells or n-wells are conventionally used in device formation see figure 1-7 of Wolf (page 11). One of ordinary skill in the art would have been motivated to use p-wells or n-wells in order to form a twin-well CMOPS structure as suggested by Wolf.

It is noted that Chow discloses the use of dummy wafers/substrates for seasoning the chamber, however, Chow is silent about using a second substrate which is not to form a device conventionally known as a dummy substrate.

Lui discloses dummy substrates are conventionally used for etch chamber cleaning (column 1, line 33).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Chow to use a dummy substrate because dummy substrates are conventionally used for etch chamber cleaning. One of ordinary skill in the art would have been motivated to use a dummy substrate in order to decouple the processes of chamber cleaning from etching when the substrate is sensitive to the cleaning byproducts. One of ordinary skill in the art would have been motivated to modify the method of Chow by performing cleaning independently of the etching step when the two processes result in undesirable effects on the substrate such as contamination or incontrollable etch, the method of Chow could obviously be extended to process more delicate substrates, by performing independent etch and clean steps.

Applicant does not specify details of the kind of etching performed in applicant's claim 29, it would appear that the chamber cleaning procedure and the etch step of

Chow would be effective regardless of whether an insulating layer is present under the conducting layer or not, etching is usually performed on the topmost layer. It would also appear obvious to one of ordinary skill in the art at the time the invention was made that the sequence of layers positioned bellow the topmost layers of conductive films would not affect the chamber cleaning step since those layers are not exposed to the cleaning environment.

As to claim 35, Unlike the instant claimed invention as per claim 35, Chow fails to disclose that BOx/residue is adhered to the surface of the quartz and etching to remove Box from the chamber Ye discloses a method for cleaning a plasma etching apparatus comprising a step of cleaning an inner surface of a chamber with chlorine containing gas to remove BOx adhered to the chamber surface (Table 1)

Since Chow is concerned with an etching step using Cl2, one skilled in the art at the time the invention was made would have found it obvious that Chow etching step would have resulted in BOx/residue adhered to the surface of the chamber in view of Ye teaching because Ye discloses that during a chlorine base etch process, non-volatile contaminants are deposited on the chamber wall/inner surface of the chamber (col 7, lines 60-67, col 8, lines 1-5). One skilled in the art at the time the invention was made would also have found it obvious to employ Chow cleaning step to remove Box from an inner surface of the chamber in view of Ye teaching because Ye discloses that the concept of using the halogenated gas mixture to remove by-products is applicable to semiconductor processing chambers in general (col 6, lines 40-45).

Regarding claim 30, Chow discloses using an ICP etching method (col 6, lines 35-40)

Regarding claim 31, Chow discloses that the fluorine gas is CF4 (col 9, lines 37-40)

The limitation of claim 32, have been discussed above, Chow discloses adding oxygen gas to the cleaning plasma (col 9, lines 37-40), fig. Id of Chow shows an island shaped semiconductor structure is formed.

Regarding claim 33, Chow discloses using a etching gas mixture of CI2, SF6 and oxygen (col 9, lines 36-51)

As to claim 34, the limitation of a quartz dummy wafer has been discussed above.

Claim Rejections - 35 USC § 103

7. Claims 36-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lu et al (US 6,352,081) in view Chow et al (US 6,872,322) Lui et al. (US 6,566,270) and Wolf (Silicon Processing for the VLSI Era, Volume 4- Deep Submicron Process Technology, Lattice Press, 2002, page 11).

8. The references of Chow, Lui and Wolf have been discussed above.

Lu discloses a method of cleaning processing chamber. The method comprises the steps of:

performing plasma etching using a gas containing BCI3 as an etching gas in the

chamber (col 9, lines 50-55), changing/replacing the etching gas with Cl2 gas after the plasma etching (col 10, lines 60-65), generating plasma from the Cl2 (col 10, lines 63- 65), the chamber includes a quartz exposed to the inside of the chamber (col 7, lines 15-20; fig. 2C)

It is noted that Lu is silent about a conductive film.

Chow discloses forming a conductive film, a silicon oxide layer under the polysilicon and tungsten layers (col 8, lines 15-17).

Chow discloses forming a silicon oxide layer under the polysilicon and tungsten layers (col 8, lines 15-17). The oxide layer of Chow is a gate oxide deposited on top of a semiconductor film which forms the channel underneath the gate, as anyone with ordinary skill in the art would know that the semiconducting channel is formed on a "first" substrate. It is noted that Chow is silent about the formation of the transistor channel including the oxide layer being deposited on a conductive layer, however Wolf teaches p-wells or n-wells are conventionally used in device formation see figure 1-7 of Wolf (page 11). One of ordinary skill in the art would have been motivated to use p-wells or n-wells in order to form a twin-well CMOPS structure as suggested by Wolf.

It is noted that Chow discloses the use of dummy wafers/substrates for seasoning the chamber, however, Lu and Chow are silent about using a second substrate which is not to form a device conventionally known as a dummy substrate for chamber cleaning.

Lui discloses dummy substrates are conventionally used for etch chamber cleaning (column 1, line 33).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the modified process of Lu to use a dummy substrate because dummy substrates are conventionally used for etch chamber cleaning. One of ordinary skill in the art would have been motivated to use a dummy substrate in order to decouple the processes of chamber cleaning from etching when the substrate is sensitive to the cleaning byproducts. One of ordinary skill in the art would have been motivated to further modify the method of Lu by performing cleaning independently of the etching step when the two processes result in undesirable effects on the substrate such as contamination or incontrollable etch, the method of Lu and Chow could obviously be extended to process more delicate substrates, by performing independent etch and clean steps.

Applicant does not specify details of the kind of etching performed in applicant's claim 36, it would appear that the chamber cleaning procedure and the etch step of Lu and Chow would be effective regardless of whether an insulating layer is present under the conducting layer or not, etching is usually performed on the topmost layer. It would also appear obvious to one of ordinary skill in the art at the time the invention was made that the sequence of layers positioned bellow the topmost layers of conductive films would not affect the chamber cleaning step since those layers are not exposed to the cleaning environment.

Regarding claim 37, Lu discloses using an ICP etching method (col 8, lines 42-45)

Regarding claims 38-39, 41, Lu discloses that the fluorine gas is CF4 (col 8, lines 49- 50), using a quartz plate in the chamber (col 8, lines 46-48)

Regarding claim 42, Lu discloses adding oxygen gas to the cleaning plasma (col 10, lines 62-64)

Claim Rejections - 35 USC § 103

9. Claims 43-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow et al (US 6,872,322) in view of Lui et al. (US 6,566,270) and Wolf (Silicon Processing for the VLSI Era, Volume 4- Deep Submicron Process Technology, Lattice Press, 2002, page 11).

10. The references of Chow, Lui and Wolf have been discussed above.

Regarding claims 43- 48, the reference of Chow has been discussed above, it discloses manufacturing a semiconductor device by forming a semiconductor film over a substrate, and a conducting film (comprising at least two conductive layers)over the semiconductor film (Column 8, lines 8-18). Chow discloses cleaning the chamber with Cl2, N2, CF4 and O2 (column 9, line 40) plasma.

It is noted that Chow is silent about an insulating film between the semiconductor layer and the first conductive layer, however, Chow discloses forming a silicon oxide layer under the polysilicon and tungsten layers (col 8, lines 15-17). The oxide layer of Chow is a gate oxide deposited on top of a semiconductor film which forms the channel underneath the gate, as anyone with ordinary skill in the art would know that the semiconducting channel is formed on a "first" substrate. It is noted that

Chow is silent about the formation of the transistor channel including the oxide layer being deposited on a conductive layer, however Wolf teaches p-wells or n-wells are conventionally used in device formation see figure 1-7 of Wolf (page 11). One of ordinary skill in the art would have been motivated to use p-wells or n-wells in order to form a twin-well CMOPS structure as suggested by Wolf. It would appear that the etching/cleaning method of Chow would be effective even when an insulating layer is present in the film stack because the cleaning chemistry would react with the chamber walls regardless of the presence or absence of an insulating intermediate layer.

Fig. Id of Chow shows an island shaped semiconductor structure is formed.

It is noted that Chow discloses the use of dummy wafers/substrates for seasoning the chamber, however, Lu and Chow are silent about using a second substrate which is not to form a device conventionally known as a dummy substrate.

Lui discloses dummy substrates are conventionally used for etch chamber cleaning (column 1, line 33).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the modified process of Lu to use a dummy substrate because dummy substrates are conventionally used for etch chamber cleaning. One of ordinary skill in the art would have been motivated to use a dummy substrate in order to decouple the processes of chamber cleaning from etching when the substrate is sensitive to the cleaning byproducts. One of ordinary skill in the art would have been motivated to further modify the method of Lu by performing cleaning independently of the etching step when the two processes result in undesirable effects

on the substrate such as contamination or incontrollable etch, the method of Lu and Chow could obviously be extended to process more delicate substrates, by performing independent etch and clean steps.

Applicant does not specify details of the kind of etching performed in applicant's claim 43, it would appear that the chamber cleaning procedure and the etch step of Lu and Chow would be effective regardless of whether an insulating layer is present under the conducting layer or not, etching is usually performed on the topmost layer. It would also appear obvious to one of ordinary skill in the art at the time the invention was made that the sequence of layers positioned bellow the topmost layers of conductive films would not affect the chamber cleaning step since those layers are not exposed to the cleaning environment.

As to claim 49, Chow discloses BCl3 and O2 are conventionally used for etching (column 8, line 50-52), hence, it would have been obvious to one of ordinary skill in the art at the time the invention was made to expect Box to be included in the chamber walls in the deposit.

As to claims 50-56, it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the cleaning after any etching step including the conductive layer first etching step or the second etching step or after the first and second etching step because Chow teaches the concept of intermediate cleaning step and Lui teaches the concept of dummy wafer cleaning step, one of ordinary skill in the art would have been motivated to fine tune a cleaning step using the teachings of Chow and Lui to enhance the etching characteristics of a layer stack with

similar materials by routine experimentation including modifying the cleaning sequence, in order to obtain the best possible results according the specific layer stack.

Claim Rejections - 35 USC § 103

11. Claims 57-63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow et al (US 6,872,322) in view of Lu et al (US 6,352,081), Lui et al. (US 6,566,270) and Wolf (Silicon Processing for the VLSI Era, Volume 4- Deep Submicron Process Technology, Lattice Press, 2002, page 11).

12. The references of Chow, Lui and Wolf have been discussed above.

Regarding claim 57, It is noted that Chow is silent about an etching step using BCl3 on a first device

Lu discloses a method of cleaning processing chamber. The method comprises the steps of:

performing plasma etching using a gas containing BCl3 as an etching gas in the chamber (col 9, lines 50-55), changing/replacing the etching gas with Cl2 gas after the plasma etching (col 10, lines 60-65), generating plasma from the Cl2 (col 10, lines 63-65) before etching with SF6/a gas that is inhibited from generating Box (col 11, lines 40-45) the chamber includes a quartz exposed to the inside of the chamber (col 7, lines 15-20; fig. 2C).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the cleaning after any etching step including

the conductive layer first etching step or the second etching step or after the first and second etching step because Chow teaches the concept of intermediate cleaning step and Lui teaches the concept of dummy wafer cleaning step, one of ordinary skill in the art would have been motivated to fine tune a cleaning step using the teachings of Chow and Lui to enhance the etching characteristics of a layer stack with similar materials by routine experimentation including modifying the cleaning sequence, in order to obtain the best possible results according the specific layer stack. It would also appear obvious to one of ordinary skill in the art at the time the invention was made that the sequence of layers positioned bellow the topmost layers of conductive films would not affect the chamber cleaning step since those layers are not exposed to the cleaning environment.

As to the limitations of forming a first semiconductor device and a second semiconductor device Chow discloses the method can be used for etching a structure as shoen in figure 1b, and also for forming a structure as shown in figure 1d.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform both types of etches in the same chamber. One of ordinary skill in the art would have been motivated to perform two types of etches in the same chamber in order to lower the manufacturing cost, Chow teaches how to reduce or eliminate undesired effects due to residuals in the chamber by performing chamber cleaning between etch steps.

As to claims 58-63, all the limitation of these claims have been discussed above.

Claim Rejections - 35 USC § 103

13. Claims 64-70 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lu et al (US 6,352,081) in view of Chow et al (US 6,872,322), Lui et al. (US 6,566,270) and Wolf (Silicon Processing for the VLSI Era, Volume 4- Deep Submicron Process Technology, Lattice Press, 2002, page 11).

14. The references of Chow, Lui and Wolf have been discussed above.

Lu discloses a method of cleaning processing chamber. The method comprises the steps of:

processing a first semiconductor device by performing plasma etching using a gas containing BCl3 as an etching gas in the chamber (col 9, lines 50-55), changing/replacing the etching gas with Cl2 gas after the plasma etching (col 10, lines 60-65), generating plasma from the Cl2 (col 10, lines 63-65) before etching with SF6/a gas. Lu teaches that changing etching gases in a chamber is conventionally used in the art of etching.

Unlike the instant claimed inventions as per claim 57, 64, Lu fails to expressly disclose manufacturing a second semiconductor device using the cleaned chamber although Lu discloses performing wafer processing runs (col 12, lines 40-42)

Chow, as discussed above, discloses a method for cleaning a plasma etching chamber comprising the steps of processing/manufacturing a second semiconductor device using the cleaned chamber (col 11, lines 14-20).

Chow discloses forming a silicon oxide layer between the polysilicon and tungsten layers (col 8, lines 15-17)

It is noted that Chow discloses the use of dummy wafers/substrates for seasoning the chamber, however, Chow is silent about using a second substrate which is not to form a device conventionally known as a dummy substrate.

Lui discloses dummy substrates are conventionally used for etch chamber cleaning (column 1, line 33).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Chow to use a dummy substrate because dummy substrates are conventionally used for etch chamber cleaning. One of ordinary skill in the art would have been motivated to use a dummy substrate in order to decouple the processes of chamber cleaning from etching when the substrate is sensitive to the cleaning byproducts. One of ordinary skill in the art would have been motivated to modify the method of Chow by performing cleaning independently of the etching step when the two processes result in undesirable effects on the substrate such as contamination or incontrollable etch, the method of Chow could obviously be extended to process more delicate substrates, by performing independent etch and clean steps.

Applicant does not specify what kind of etching in performed in applicant's claim 64, it would appear that the chamber cleaning procedure and the etch step of Chow would be effective regardless of whether an insulating layer is present under the conducting layer or not, etching is usually performed on the topmost layer. It would also appear obvious to one of ordinary skill in the art at the time the invention was made that the sequence of layers positioned bellow the topmost layers of conductive films would

not affect the chamber cleaning step since those layers are not exposed to the cleaning environment.

One skilled in the art at the time the invention was made would have found it obvious to modify Lu method by manufacturing a second semiconductor device using the cleaned chamber because it is conventional in the art as taught by Chow

Regarding claim 65, Lu discloses using an ICP etching method (col 8, lines 42-45)

Regarding claims 66, 67, 70, Lu discloses that the fluorine gas is CF4 (col 8, lines 49-50), using a quartz plate in the chamber (col 8, lines 46-48)

Regarding claim 68, Lu discloses adding oxygen gas to the cleaning plasma (col 10, lines 62-64)

Claim Rejections - 35 USC § 103

15. Claims 71-84 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lu et al (US 6,352,081) in view of Izawa et al (US 6,842,658) and further in view of Chow et al (US 6,872,322) and Wolf (Silicon Processing for the VLSI Era, Volume 4- Deep Submicron Process Technology, Lattice Press, 2002, page 11).

The references of Chow, Lu and Wolf have been discussed above.

Lu discloses a method of cleaning processing chamber. The method comprises the steps of:

performing plasma etching using a gas containing BCl3 as an etching gas in the chamber (col 9, lines 50-55), changing/replacing the etching gas with Cl2 gas after the plasma etching (col 10, lines 60-65), generating plasma from the Cl2 (col 10, lines 63-65) before etching with SF6/a gas that is inhibited from generating Box (col 11, lines 40-45) the chamber includes a quartz exposed to the inside of the chamber (col 7, lines 15-20; fig. 2C)

Izawa discloses a method of manufacturing a semiconductor device comprises a step of applying a dielectric magnetic field generated from the electrode through the quartz adjacent the electrode (col 8, lines 50-54; fig. 3).

Lu fails to expressly disclose manufacturing a second semiconductor device using the cleaned chamber although Lu discloses performing wafer processing runs (col 12, lines 40-42)

Chow discloses a method for cleaning a plasma etching chamber comprising the steps of processing/manufacturing a second semiconductor device using the cleaned chamber (col 11, lines 14-20)

One skilled in the art at the time the invention was made would have found it obvious to modify Lu method by manufacturing a second semiconductor device using the cleaned chamber because it is conventional in the art as taught by Chow.

It is noted that Lu is silent about the exact film stack as described in applicant's claim 71. The film stack of Chow has been described above.

Applicant does not specify details about the kind of etching performed in applicant's claim 71, it would appear that the chamber cleaning procedure and the etch

step of Chow would be effective regardless of whether an insulating layer is present under the conducting layer or not, etching is usually performed on the topmost layer. It would also appear obvious to one of ordinary skill in the art at the time the invention was made that the sequence of layers positioned bellow the topmost layers of conductive films would not affect the chamber cleaning step since those layers are not exposed to the cleaning environment.

Regarding claim 72, 79, Lu discloses using an ICP etching method (col 8, lines 42-45)

Regarding claim 73, 74, 80, 81, 83, Lu discloses that the fluorine gas is CF4 (col 8,lines 49-50), using a quartz plate in the chamber (col 8, lines 46-48)

Regarding claims 75, 82, Lu discloses adding oxygen gas to the cleaning plasma (col 10, lines 62-64)

Claims 77, 84 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lu et al (US 6,352,081) in view of Izawa et al (US 6,842,658) and further in view of Chow et al (US 6,872,322) and Ye et al (US 5,756,400) based on the ground of rejection set forth in paragraphs 13-15 above.

Claim Rejections - 35 USC § 103

16. Claims 6,14, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow et al (US 6,872,322) in view of Lui et al. (US 6,566,270) and Ye et al (US 5,756,400) and Wolf (Silicon Processing for the VLSI Era, Volume 4- Deep Submicron Process Technology, Lattice Press, 2002, page 11).

Chow method has been described above. Unlike the instant claimed invention as per claim 6, Chow fails to disclose cleaning includes removing BOx from an inner surface of the chamber

Ye discloses a method for cleaning a plasma etching apparatus comprising a step of cleaning an inner surface of a chamber with chlorine containing gas to remove BOx (Table 1)

Since Chow is directed to a step of cleaning a chamber using chlorine containing gas, one skilled in the art at the time the invention was made would have found it obvious to employ Chow cleaning step to remove Box from an inner surface of the chamber in view of Ye teaching because Ye discloses that the concept of using the halogenated gas mixture to remove by-products is applicable to semiconductor processing chambers in general (col 6, lines 40-45)

Claim Rejections - 35 USC § 103

17. Claims 42, 49, 56, 62, 69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lu et al (US 6,352,081) in view of Izawa et al (US 6,842,658) and further in view of Ye et al (US 5,756,400) and Wolf (Silicon Processing for the VLSI Era, Volume 4- Deep Submicron Process Technology, Lattice Press, 2002, page 11).

Lu as modified by Izawa has been described above. Unlike the instant claimed invention as per claim 42, 49, 56, 62, 69, Lu and Izawa fails to disclose cleaning includes removing BOx from an inner surface of the chamber Ye discloses a method

for cleaning a plasma etching apparatus comprising a step of cleaning an inner surface of a chamber with chlorine containing gas to remove BOx (Table 1)

Since Lu is directed to a step of cleaning a chamber using chlorine containing gas, one skilled in the art at the time the invention was made would have found it obvious to employ Lu and Izawa cleaning step to remove Box from an inner surface of the chamber in view of Ye teaching because Ye discloses that the concept of using the halogenated gas mixture to remove by-products is applicable to semiconductor processing chambers in general (col 6, lines 40-45)

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 4, 5, 7, 8, 9, 11, 12, 13, are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoefler et al. (US 2003/0222306) in view of Yeh et al. (US 2002/0162827).

Regarding Claims 1, 2, 5, 7, 8, 9, 11, 12, Hoefler discloses a method for manufacturing a semiconductor device, the method comprising: forming a semiconductor film (18) over a first substrate; forming an insulating film (32) over the semiconductor film; forming a conductive film (34) over the semiconductor insulating film; the conductive layer is etched (figure 4 to figure 5).

It is noted Hoefler is silent about cleaning a chamber, the cleaning including comprising: placing a second substrate in the chamber, wherein said second substrate is not to form a semiconductor device; filling the chamber with a cleaning gas, said cleaning gas comprising Cl2 or a mixed gas of Cl2 and a fluorine-based gas; and generating plasma from the cleaning gas; placing the first substrate with the conductive film, the insulating film and the semiconductor film in the cleaned chamber; and etching the conductive film in the cleaned chamber.

Yeh teaches a conductive etch chamber cleaning method wherein "The method further comprises the step of generating a plasma by applying RF energy to the first and second cleaning process gases, such as oxygen and chlorine gases, ... If there is a sacrificial substrate (also known as a dummy wafer) positioned on the substrate holder 118 to protect the holder 118 from damage during the plasma cleaning operation, the power applied to the second electrode can be set between about 100 W and about 250W. Thus, the method is feasible at the wafer/waferless condition. The method further comprises the step of evacuating the first cleaning process gas from the chamber 100 between the first and the second time periods while maintaining the plasma" (paragraph 0027).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Hoefler by including a chamber cleaning step as described by Yeh because chamber cleaning with a dummy wafer is conventionally used in the art of conductor etch. One of ordinary skill in the art would

have been motivated to include a chamber cleaning step as described by Yeh in order to achieve high yield and maintain throughput.

As to claims 4,13, it is noted that Hoefler is silent about a glass or quartz dummy wafer for the cleaning step, however, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Hoefler to use a dummy substrate made of any material including glass or quartz wich is compatible with the chamber and process chemistry because a dummy wafer is used only during cleaning. One of ordinary skill in the art would have been motivated to use glass or quartz in order to prevent introducing impurities in the chamber since glass or quartz (SiO2) is conventionally used as a material for gate material, also quartz is resistant to the cleaning chemistry, and glass or quartz wafers are readily available as dummy wafers.

Claim Rejections - 35 USC § 103

Claims 3, 6, 10, 14, are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoefler et al. (US 2003/0222306) in view of Yeh et al. (US 2002/0162827) and further in view of Nallan et al. (US 2002/0137352) and Gabriel et al. (US 6,815,359).

It is noted that Hoefler and Yeh are silent about a fluorine containing gas for cleaning.

Nallan discloses "The use of the fluorine-containing etchant in combination with the more standard chlorine-comprising agent helps remove byproducts from the etch chamber walls, keeping the chamber walls cleaner".

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify the process of Hoefler by adding CF4, NF3 or SF6 because Nallan teaches such mixtures are effective in removing byproducts from the etch chamber walls, keeping the chamber walls cleaner. One of ordinary skill in the art would have been motivated to add CF4, NF3 or SF6 in order to accelerate chamber cleaning when the chamber wall deposit contains silicon.

Yeh teaches polymer is removed with oxygen and Gabriel teaches "plasma etchant, such as, Cl.sub.2 /HBr-based plasmas for etching silicon-based conductors, Cl.sub.2 /BCl.sub.3 -based plasmas for etching metals, C.sub.4 F.sub.8 /O.sub.2 -based plasmas for etching inorganic dielectrics" (column 5, line 67)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to expect the chamber deposits to contain BOx when the etched top conductor is a metal because Gabriel teaches BCl3 is conventionally used for metal conductor etching, and Yeh suggests contaminant deposits are accumulated during etching from the etch process. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to expect BOx as contaminants when BCl3 and oxygen are used in the etch/clean processes.

Claim Rejections - 35 USC § 103

Claims 15-21, 22-28, are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoefler et al. (US 2003/0222306) in view of Yeh et al. (US 2002/0162827) and Suzawa et al. (US 2002/0171085).

Hoefler discloses "After forming and, optionally, patterning the gate dielectric 32, a conductive layer 34 is deposited by PVD, CVD, ALD, the like or combinations of the above. The conductive layer 34 is formed over both the logic region 21 and the NVM region 23 and portions of the conductive layer 34 will remain in each region after being patterned (e.g. etched). The conductive layer 34 can be any conductive material" (paragraph 0021).

It is noted Hoefler does not expressly disclose tungsten.

Suzawa teaches tungsten is a conductive material, citing ""Further, in the case where W (tungsten) film is used as the metal layer 1002a, by using a mixture gas of Cl.sub.2 (gas flow rate of 25 sccm) and CF.sub.4 (gas flow rate of 25 sccm) and O.sub.2 (gas flow rate of 10 sccm) or a mixture gas of Cl.sub.2 (gas flow rate of 12 sccm) and SF.sub.6 (gas flow rate of 6 sccm) and O.sub.2 (gas flow rate of 12 sccm) as an etching gas" (paragraph 0039).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Hoefler to include tugsten as the conductive material and etch it by using Cl.sub.2 (gas flow rate of 12 sccm) and SF.sub.6 (gas flow rate of 6 sccm) and O.sub.2 (gas flow rate of 12 sccm) as an etching gas since the prodedure is conventionally used in semiconductor processing. One of

ordinary skill in the art would have been motivated to use tungsten in order to obtain a highly conductive film.

As to claims 7, 24, see rejection of claims 3, 10, further in view of Nallan et al. (US 2002/0137352) above.

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 5, 7, 8, 9, 11, 12, 29, 30, 32, 50, 51, are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (US 2002/0048829) in view of Yeh et al. (US 2002/0162827).

Regarding Claims 1, 2, 5, 7, 8, 9, 11, 12, 29, 30, 32, 50, 51, Yamazaki discloses a method for manufacturing a semiconductor device, the method comprising: forming a semiconductor film (101) over a first substrate (100); forming an insulating film (102) over the semiconductor film; forming conductive film(s) (103/104) over the semiconductor insulating film; the conductive layer is etched (paragraph 0012).

It is noted Yamazaki is silent about cleaning a chamber, the cleaning including comprising: placing a second substrate in the chamber, wherein said second substrate is not to form a semiconductor device; filling the chamber with a cleaning gas, said cleaning gas comprising Cl2 or a mixed gas of Cl2 and a fluorine-based gas; and

generating plasma from the cleaning gas; placing the first substrate with the conductive film, the insulating film and the semiconductor film in the cleaned chamber; and etching the conductive film(s) in the cleaned chamber.

Yeh teaches a conductive etch chamber cleaning method wherein "The method further comprises the step of generating a plasma by applying RF energy to the first and second cleaning process gases, such as oxygen and chlorine gases, ... If there is a sacrificial substrate (also known as a dummy wafer) positioned on the substrate holder 118 to protect the holder 118 from damage during the plasma cleaning operation, the power applied to the second electrode can be set between about 100 W and about 250W. Thus, the method is feasible at the wafer/waferless condition. The method further comprises the step of evacuating the first cleaning process gas from the chamber 100 between the first and the second time periods while maintaining the plasma" (paragraph 0027).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Yamazaki by including a chamber cleaning step as described by Yeh because chamber cleaning with a dummy wafer is conventionally used in the art of conductor etch. One of ordinary skill in the art would have been motivated to include a chamber cleaning step as described by Yeh in order to achieve high yield and maintain throughput as suggested by Yeh. It would have been obvious to one of ordinary skill in the art at the time the invention was made, willing to accept the additional cleaning time, to perform the chamber cleaning step after each etch step. One of ordinary skill in the art would have been motivated to include a

chamber cleaning step after each of the etching steps in order to achieve high yield and maintain throughput as suggested by Yeh.

Claim Rejections - 35 USC § 103

Claims 4, 13, 34, are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (US 2002/0048829) in view of Yeh et al. (US 2002/0162827) and Saito et al. (US 6,221,200).

As to claims 4,13, it is noted that Yamazaki is silent about a glass or quartz dummy wafer for the cleaning step, Saito discloses "In order to solve the above problems, there was proposed a method which comprises fixing, in a plasma etching chamber, a material resistant to plasma etching as a dummy for a wafer, and generating a plasma in the chamber to remove the deposited silicon, etc. by etching. As the material resistant to plasma etching, usable as a dummy for a wafer, there were studied quartz, silicon carbide, graphite and the like" (column 2, line 5), it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Yamazaki to use a dummy substrate made of any material including glass or quartz wich is compatible with the chamber and process chemistry because a dummy wafer is used only during cleaning. One of ordinary skill in the art would have been motivated to use glass or quartz in order to prevent introducing impurities in the chamber since glass or quartz (SiO2) is conventionally used as a material for gate material, also quartz is resistant to the cleaning chemistry, and glass or quartz wafers are readily available as dummy wafers.

Claim Rejections - 35 USC § 103

Claims 3, 6, 10, 14, 31, 33, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, and 64-84, are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (US 2002/0048829) in view of Yeh et al. (US 2002/0162827) and further in view of Nallan et al. (US 2002/0137352) and Gabriel et al. (US 6,815,359).

Yamazaki shows multiple devices are formed on the same substrate (figures 3(A-D).

It is noted that Yamazaki and Yeh are silent about a fluorine containing gas for cleaning.

Nallan discloses "The use of the fluorine-containing etchant in combination with the more standard chlorine-comprising agent helps remove byproducts from the etch chamber walls, keeping the chamber walls cleaner".

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify the process of Yamazaki by adding CF4, NF3 or SF6 because Nallan teaches such mixtures are effective in removing byproducts from the etch chamber walls, keeping the chamber walls cleaner. One of ordinary skill in the art would have been motivated to add CF4, NF3 or SF6 in order to accelerate chamber cleaning when the chamber wall deposit contains silicon.

It is noted Yamazaki is silent about BOx or etching with BCl3.

Yeh teaches polymer is removed with oxygen and Gabriel teaches "plasma etchant, such as, Cl.sub.2 /HBr-based plasmas for etching silicon-based conductors, Cl.sub.2 /BCl.sub.3 -based plasmas for etching metals, C.sub.4 F.sub.8 /O.sub.2 -based plasmas for etching inorganic dielectrics" (column 5, line 67)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to expect the chamber deposits to contain BOx when the etched top conductor is a metal because Gabriel teaches BCl3 is conventionally used for metal conductor etching, and Yeh suggests contaminant deposits are accumulated during etching from the etch process. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to expect BOx as contaminants when BCl3 and oxygen are used in the etch/clean processes.

As to claims 39, 41, 48, 49, 53, 55, 56, 63, see rejection in view of Saito et al. (US 6,221,200) above.

Response to Arguments

20. Applicant's arguments filed 3/2/2007 have been fully considered but they are not persuasive.

Regarding applicant's argument stating "Chow, a single substrate (which forms the semiconductor device) remains in the chamber during the cleaning stage and there is no suggestion that cleaning of the chamber includes placing a dummy or second substrate in the chamber" and "Chow explicitly teaches away from such a second or dummy substrate and explains that increased cost is associated with additional

substrates "that results from the downtime of the etching chamber during the dry or wet cleaning and seasoning process steps". The examiner maintains that, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Chow to use a dummy substrate because dummy substrates are conventionally used for etch chamber cleaning because Lui discloses dummy substrates are conventionally used for etch chamber cleaning (column 1, line 33). One of ordinary skill in the art would have been motivated to use a dummy substrate in order to decouple the process of chamber cleaning from the process of etching when the substrate is sensitive to the cleaning byproducts. One of ordinary skill in the art would have been motivated to modify the method of Chow by performing cleaning independently of the etching step when the cleaning process result in undesirable effects on the substrate such as contamination or incontrollable etch, the method of Chow could obviously be extended to process more delicate substrates, by performing independent etch and clean steps. Lui teaches cleaning the chamber using a dummy wafer on the chuck while cleaning.

Chow does not teach away from such a second or dummy substrate, Chow on the contrary, Chow teaches it is desirable to dry clean the chamber preferably at the same time the etching is performed, however, if the time necessary for cleaning the chamber is longer than the etching time, damage can result from the over-etching on the substrate. Chow teaches "it is desirable to have an etch process that reduces formation of etchant residue in the etching chamber" (column 3, line 28), if the residue removal is not as fast as the etching, cleaning the chamber through dry or wet cleaning

is still necessary according to Chow. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Chow to perform the dry cleaning in a separate step as suggested by Lui. When it comes to deciding between downtime of the etching chamber during the dry or wet cleaning and damage that can result from the over-etching on the substrate, the examiner maintains that it would have been obvious to one of ordinary skill in the art at the time the invention was made to chose performance of the resulting devices rather than a shorter overall process yielding impractical damaged devices.

As to applicant's argument about claim 64, as discussed in the office action Lui discloses dummy substrates are conventionally used for etch chamber cleaning, in order to introduce a dummy substrate one would have to at least interrupt the gas flow in the chamber to prevent reactive gases from filling a transfer chamber during wafer transfer, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Chow to use a cleaning gas mixture that is different than the etching gas mixture if a different gas mixture is more effective in cleaning the chamber. In addition, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Chow to use a different second etching gas for etching a different layer when a different layer needs to be etched.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mahmoud Dahimene whose telephone number is (571) 272-2410. The examiner can normally be reached on week days from 8:00 AM. to 5:00 PM..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MD.

Nadine Norton
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Art Unit 1765